CLAIMS:

1. A computer system comprising:

at least one dense logic device;

a controller for coupling said at least one dense logic device to a control block and a memory bus;

one or more memory module slots coupled to said memory bus;

an adapter port associated with a subset of said one or more memory module slots, said adapter port including associated memory resources; and

at least one direct execution logic element coupled to said adapter port, said memory resources being selectively accessible by said at least one dense logic device and said at least one direct execution logic element.

2. The computer system of claim 1 wherein said controller comprises an interleaved memory controller.

3. The computer system of claim 1 wherein said plurality of memory module slots comprise DIMM memory module slots.

4. The computer system of claim 3 wherein said adapter port comprises a DIMM physical format for retention within one of said DIMM memory module slots.

5. The computer system of claim 1 wherein said plurality of memory module slots comprise RIMM memory module slots.

6. The computer system of claim 5 wherein said adapter port comprises a RIMM physical format for retention within one of said RIMM memory module slots.

7. The computer system of claim 1 wherein said control block provides control information to said adapter port.

8. The computer system of claim 1 wherein said control block provides control information to said direct execution logic element.

9. The computer system of claim 1 wherein said control block comprises a peripheral bus control block.

10. The computer system of claim 9 wherein said peripheral bus control block provides control information to said adapter port.

11. The computer system of claim 9 wherein said peripheral control block provides control information to said direct execution logic element.

12. The computer system of claim 1 wherein said control block comprises a graphics control block.

13. The computer system of claim 12 wherein said graphics control block provides control information to said adapter port.

14. The computer system of claim 12 wherein said graphics control block provides control information to said direct execution logic element.

15. The computer system of claim 1 wherein said control block comprises a systems maintenance control block.

16. The computer system of claim 15 wherein said systems maintenance control block provides control information to said adapter port.

17. The computer system of claim 15 wherein said systems maintenance control block provides control information to said direct execution logic element.

18. The computer system of claim 1 wherein said direct execution logic element comprises a reconfigurable processor element.

19. The computer system of claim 1 wherein said direct execution logic element is operative to alter data received from said controller on said memory bus.

20. The computer system of claim 1 wherein said direct execution logic element is operative to alter data received from an external source prior to placing altered data on said memory bus.

21. The computer system of claim 1 wherein said direct execution logic element comprises:

a control block coupled to said adapter port.

22. The computer system of claim 21 wherein said direct execution logic element further comprises:

at least one field programmable gate array configurable to perform an identified algorithm on and operand provided thereto by said adapter port.

23. The computer system of claim 22 further comprising:

a dual-ported memory block coupling a control block coupled to said adapter port to said at least one field programmable gate array.

24. The computer system of claim 1 wherein said direct execution logic element comprises:

a chain port for coupling said direct execution logic element to another direct execution logic element.

25. The computer system of claim 21 wherein said direct execution logic element further comprises:

a read only memory associated with said control block for providing configuration information thereto.

26. A computer system comprising:

at least one dense logic device;

an interleaved controller for coupling said at least one dense logic device to a control block and a memory bus;

a plurality of memory slots coupled to said memory bus;

an adapter port associated with at least two of said plurality of memory slots, each of said adapter port including associated memory resources; and

a direct execution logic element coupled to at least one of said adapter ports, said memory resources being selectively accessible by said at least one dense logic device and said direct execution logic element.

27. The computer system of claim 26 wherein said plurality of memory slots comprise DIMM memory module slots.

28. The computer system of claim 27 wherein said adapter port comprises a DIMM physical format for retention within one of said DIMM memory module slots.

29. The computer system of claim 26 wherein said plurality of memory slots comprise RIMM memory module slots.

30. The computer system of claim 29 wherein said adapter port comprises a RIMM physical format for retention within one of said RIMM memory module slots.

31. The computer system of claim 26 wherein said control block provides control information to said adapter port.

32. The computer system of claim 26 wherein said control block provides control information to said direct execution logic element.

33. The computer system of claim 26 wherein said control block comprises a peripheral bus control block.

34. The computer system of claim 33 wherein said peripheral bus control block provides control information to said adapter port.

35. The computer system of claim 33 wherein said peripheral control block provides control information to said direct execution logic element.

36. The computer system of claim 26 wherein said control block comprises a graphics control block.

37. The computer system of claim 36 wherein said graphics control block provides control information to said adapter port.

38. The computer system of claim 36 wherein said graphics control block provides control information to said direct execution logic element.

39. The computer system of claim 26 wherein said control block comprises a systems maintenance control block.

40. The computer system of claim 39 wherein said systems maintenance control block provides control information to said adapter port.

41. The computer system of claim 39 wherein said systems maintenance control block provides control information to said direct execution logic element.

42. The computer system of claim 26 wherein said control block comprises a PCI-X control block.

43. The computer system of claim 42 wherein said PCI-X control block provides control information to said adapter port.

44. The computer system of claim 42 wherein said PCI-X control block provides control information to said direct execution logic element.

45. The computer system of claim 26 wherein said control block comprises a PCI Express control block.

46. The computer system of claim 45 wherein said PCI Express control block provides control information to said adapter port.

47. The computer system of claim 45 wherein said PCI Express control block provides control information to said direct execution logic element.

48. The computer system of claim 26 wherein said direct execution logic element comprises a reconfigurable processor element.

49. The computer system of claim 26 wherein said direct execution logic element is operative to alter data received from said controller on said memory bus.

50. The computer system of claim 26 wherein said direct execution logic element is operative to alter data received from an external source prior to placing altered data on said memory bus.

51. The computer system of claim 26 wherein said direct execution logic element comprises:

a control block coupled to said adapter port.

52. The computer system of claim 51 wherein said direct execution logic element further comprises:

at least one field programmable gate array configurable to perform an identified algorithm on and operand provided thereto by said adapter port.

53. The computer system of claim 52 further comprising:

a dual-ported memory block coupling a control block coupled to said adapter port to said at least one field programmable gate array.

54. The computer system of claim 26 wherein said direct execution logic element comprises:

a chain port for coupling said processor element to another direct execution logic element.

55. The computer system of claim 51 wherein said direct execution logic element further comprises:

a read only memory associated with said control block for providing configuration information thereto.

56. A computer system including an adapter port for electrical coupling between a memory bus of said computer system and a network interface, said computer system comprising at least one dense logic device coupled to said memory bus, said adapter port comprising:

a memory resource associated with said adapter port; and

a control block for selectively enabling access by said at least one dense logic device to said memory resource.

57. The computer system of claim 56 wherein said control block is further operational to selectively preclude access by said at least one dense logic device to said memory resource.

58. The computer system of claim 56 further comprising:

at least one direct execution logic element coupled to said network interface.

59. The computer system of claim 58 wherein said control block is further operational to alternatively enable access to said memory resource by said at least one dense logic device and said at least one direct execution logic element.

60. The computer system of claim 56 wherein said memory bus further comprises at least one memory module slot and said adapter port is configured for

physical retention within said at least one memory module slot.

61. The computer system of claim 60 wherein said at least one memory module slot comprises a DIMM slot.

62. The computer system of claim 60 wherein said at least one memory module slot comprises a RIMM slot.

63. The computer system of claim 56 further comprising:

an additional adapter port;

an additional memory resource associated with said additional adapter port, said control block further operative to selectively enable access by said at least one dense logic device to said additional memory resource.

64. The computer system of claim 63 wherein said control block is further operational to selectively preclude access by said at least one dense logic device to said memory resource and said additional memory resource.

65. The computer system of claim 64 further comprising at least one direct execution logic element coupled to said network interface.

66. The computer system of claim 65 wherein said control block is further operational to alternatively enable access to said memory resource and said additional memory resource by said at least one dense logic device and said at least one direct execution logic element.

67. The computer system of claim 63 wherein said memory bus further comprises first and second memory module slots for physical retention of said at least one adapter port and said additional adapter port respectively.

68. The computer system of claim 67 wherein said first and second memory module slots comprise DIMM slots.

69. The computer system of claim 67 wherein said first and second memory module slots comprise RIMM slots.

70. The computer system of claim 63 wherein said control block is located on a module comprising said adapter port.

71. The computer system of claim 56 wherein said computer system further comprises:

a memory and I/O controller interposed between said at least one dense logic device and said memory bus.

72. The computer system of claim 71 wherein said memory and I/O controller comprises an interleaved memory controller.

73. The computer system of claim 56 wherein said adapter port comprises a number of switches interposed between said memory bus and said memory resource controllable by said control block.

74. The computer system of claim 73 wherein said switches comprise field effect transistors.

75. The computer system of claim 73 wherein said switches have a first condition thereof for coupling said dense logic device to said memory resource and a second condition thereof for coupling said network interface to said memory resource.

76. The computer system of claim 56 wherein said memory bus comprises address/control and data portions thereof.

77. The computer system of claim 56 wherein said memory bus provides address/control and data inputs to said control block to at least partially control its functionality.

78. The computer system of claim 56 wherein said control block further comprises a DMA controller for providing direct memory access operations to said memory resource.

79. The computer system of claim 78 wherein said DMA controller is fully parameterized.

80. The computer system of claim 78 wherein said DMA controller enables scatter/gather functions to be implemented.

81. The computer system of claim 78 wherein said DMA controller enables irregular data access pattern functions to be implemented.

82. The computer system of claim 78 wherein said DMA controller enables data packing functions to be implemented.

83. The computer system of claim 56 wherein said memory resource may be isolated from said memory bus in response to said control block to enable access thereto by a device coupled to said network interface.

84. The computer system of claim 56 wherein said memory resource comprises random access memory.

85. The computer system of claim 84 wherein said random access memory comprises DRAM.